The
3380P
IC Tester Specification

The Index Table:

The systems 3
The system structure, pin count, and configuration 4
The system structure, pin count, and configuration (Continue) 5
The Mechanical Specification: 6
The MXPG3 (sequence controller) specification 7
The MXLPC (64 IO Pin) AC Specification Summary 8
The MXLPC DC specification summary 11
The MXLPC HSTMU specification 14
The MXDPS (Device Power Supply) specification 15
The MLDPS (Device Power Supply) specification summary 18
The MXPMU (Precision Measurement Unit) specification summary 20
The MXREF (Reference Power Source) specification summary 21
The MXUVI (Universal Voltage/Current Source) specification summary 23
The MXAWI (ADDA) specification summary 25
The MAWI2 (ADDA) specification summary 26
The MXBUS board: 29
The STPCI board: 29
The STPHI Board: 29
The PXI extension carriage board: 29

The systems

1. Configuration:

Test head:	All AC+DC board
Manipulator:	For test head
Mainframe:	none
Controller:	PC
Controller OS:	Microsoft Windows 7
Associate and option:	GPIB, PHI, ALPG, Scan

2. The AC Power requirement:

Model	3380P Logic Tester
AC Input Rating Voltage:	200 - 240V +-10% V_{LL} 47 - 63 Hz 3 phase with 4 wires, or single phase with 3 wires
KVA:	3.0 KVA, continue

3. The environment:

Temperature	Operating: +20°C ~ +26°C Storage: -20 °C ~ +50°C Change rate: Re-calibration are require while temperature change more than +/- 1 °C
Humidity	Operating: 50% ~ 70% Storage: 20% ~ 90%
Maximum air Flow Test Head	Average: 30 CMM

4. The Control PC requirement:

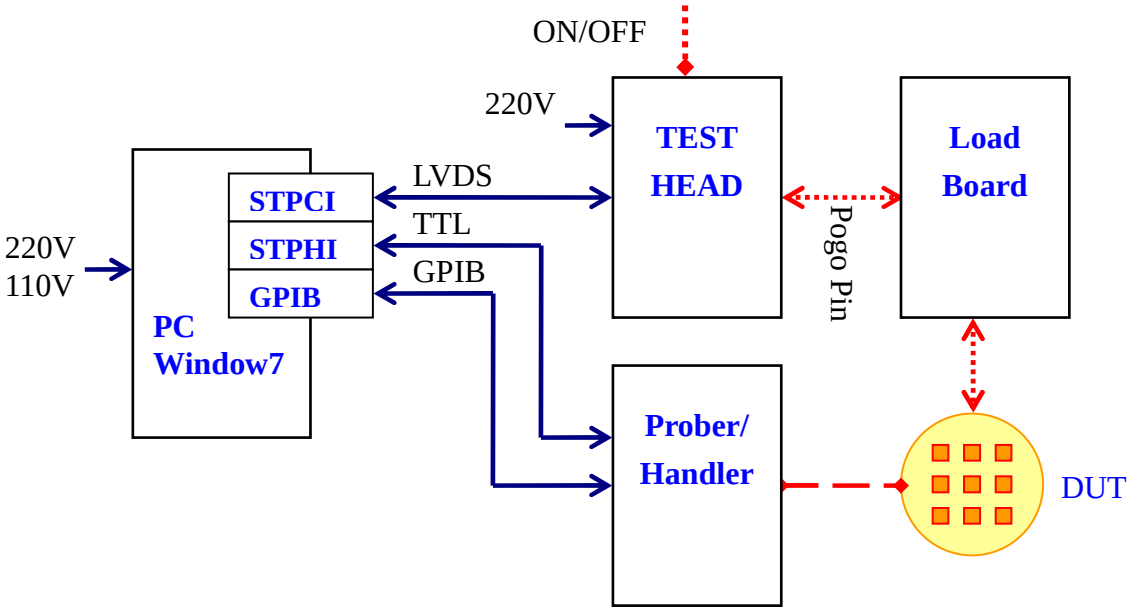
PCI 2.0 Slot	*2, for STPCI, and STPHI
PCIe Slot	*2, for GPIB, or others option

The system structure, pin count, and configuration

1. The system structure:

- The system included test head, manipulator, and a control PC.
- The test head provide room for all electronic board and power supply unit. Everything in one box
- The manipulator incorporates with test head to dock to prober or handler.
- The control PC runs with Microsoft Windows 7 OS.
- The software package “CRAFT” is special development for 3380/3380P IC tester operation.

2. The system connection diagram:



The system structure, pin count, and configuration (Continue)

3. The pin count configuration (in test head):

	Model Name	Logic Tester	Notes
Configuration	IO Pin No.	512	
	PMU Ch No.	16	
	DPS Ch. No.	8	
Boards Installation	MXLPC	8	64 pin per board
	MXPMU	1	16 channel per board
	MXDPS	1	8 channel per board
	MXPG3	1	
	MXBUS	1	
	(Empty)	1	Option, TBD
Interface	STPCI	1	
	STPHI	1	option

4. Resolution Summary:

Board Name	DAC Resolution	ADC Resolution	Notes
MXLPC	PE : 14 bits PPMU:16 Bits	PPMU:16 Bits	
MXPMU	16 Bits	16 Bits	
MXUVI	16 Bits	16 Bits	
MXREF	16 Bits	16 Bits	
MXDPS	16 Bits	18 Bits	
MLDPS	16 Bits	18 Bits	
MXAWI	16 Bits	16 Bits	

5. The PCB slots assign:

- 2 special purpose slots for system control → MXBUS, MXPG3.
- 1 general purpose slot for PMU → MXPMU
- 1 general purpose slot for DPS → MXDPS, MXUVI, MXREF, MLDPS.
- 9 general purpose slot → MXLPC, MXDPS, MXUVI, MXREF, MLDPS, MXAWI, MAWI2.

The Mechanical Specification:

1. Test Head:

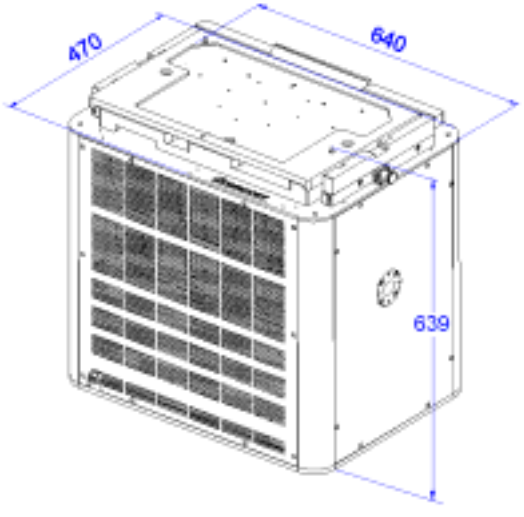
- Cable mount DUT interface approach.
- The dimension is: 640mm(width) * 470mm(Depth) *639mm(Height)
- Weight :

  > Empty T/H (Without PCB & power supply) is 55Kg

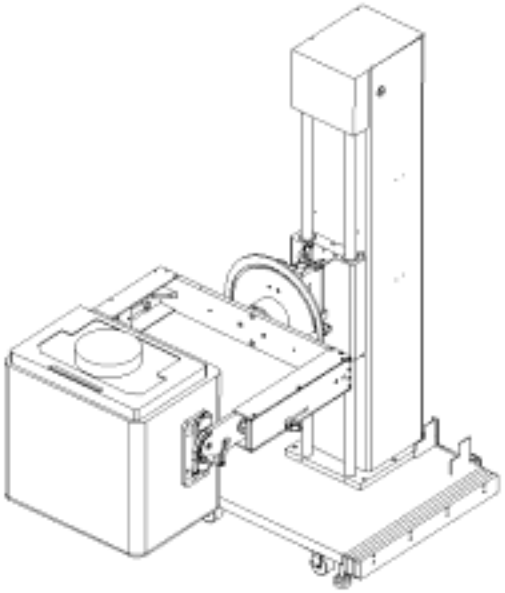
  > Fully configuration T/H (With PCB, 512pins default configuration) is 100Kg.

  > Manipulator is 350Kg, (without counterweight).
- Totally 13 slots.

2. Pictures:



Test Head



Test hard mount on manipulator

The MXPG3 (sequence controller) specification

1. Sequence controller:

Sequence control memory:	FPM: 1K SPM: 16 mega Default 32 mega Option SPM,2X mode : 32M, 64M
Multi-site support:	512 Site / System
Match mode:	Immediate match.
micro instruction support:	Refer to language for detail.
Log memory size:	1K

Note: SPM: sequential pattern memory
FPM: fast pattern memory

2. ALPG (option):

Pattern memory size:	1K
Pattern bits	16 bits X Address 16 bits Y Address 16 bits Z Data
Multi-site support:	(Same as logic pattern)

The MXLPC (64 IO Pin) AC Specification Summary

1. Configuration:

Pin number per board	64 pins / board
Maximum pattern rate:	100Mhz
Controller:	3380 MXPG3
Default pattern memory size:	32 Mega
PE Level DAC	14 Bits
PPMU Level DAC & ADC	16 Bits

2. Pattern Generator:

FPM Pattern Memory: (Fast Pattern Memory)	1K deep Normal and ALPG UI support
SPM Pattern Memory: (Sequential pattern memory) User available Pattern Memory Size: Pattern memory reserved for system: Maximum pattern rate	32M, or 64M(2X mode) 31M, or 62M (2X mode) 1M or 2M (2X mode). 100Mhz (2X mode); 50Mhz (DBL mode);
ALPG Pattern Memory configuration Pattern Memory Size: Pattern Memory width Maximum pattern rate	Option, Embedded in MXLPC 1K, remapped from FPM pattern memory *16X Address/*16Y Address/*16Data 25Mhz
SCAN Pattern Memory configuration Scan Chain Number Scan Pattern Memory Size Maximum pattern rate	Option, Embedded in MXLPC 2,4,8,16 scan chain / Board, configurable 1G bits per chain (default), 2G bits per chain (option) 50Mhz
BPM Pattern Memory: (Burst pattern memory) Pattern Memory Size: Maximum pattern rate:	Option, No SQPG micro-instruction support 32M, or 64M (2X mode) 100Mhz (2X mode); 50Mhz (DBL mode);

3. Log memory:

Fail log Memory : Memory Size: Log information: Maximum data rate:	 1K, PEH, PEL, Pin fail; 100Mhz
Capture Memory(Internal Mode) Memory deep Size: Capture information Maximum data rate: Trigger:	Re-configure from fail log memory 8k per pin, 64K maximum (8 pins in Cascade). 1 bit / pin, PEL/PEH/PFAIL selectable, 50Mhz SQPG Fail-log, or Pattern Symbol K
Capture Memory(External Mode) Memory deep Size: Capture information Maximum data rate: Trigger:	By dedicated memory device 16M per pin, 1 bit / pin, PEL/PEH/PFAIL selectable, 5Mhz SQPG Fail-log, or Pattern Symbol K

4. Timing Generator:

Timing generator scheme: Driver marker edge Strobe marker edge IO marker edge	8 edges /Pin. 4 edges/pin, 2 edges/pin, 2 edges/pin,
Number of timing set:	16 sets;
Edge setting range:	0 ns ~ (2cycle – 1.25ns)
Edge placement accuracy (EPA)	+/- 500ps
Rate setting range:	10ns to 5ms (19 bits)
Rate setting resolution:	625ps

5. Free run clock generator:

Timing generator scheme:	8 clock/board
Marker number:	2 edges / clock
Maximum clock rate:	200Mhz
Edge setting range:	0 ns ~ (1rate – 1.25ns)
Rate Setting range:	5ns to 5ms (19 bits)
Rate Setting Accuracy:	625ps

6. Pins function:

Driver waveform format:	NRZ, RO, RZ, 1, 0, SBC, DNRZ.
Compare marker type:	Edge, Window strobe (minimum tw=20ns);
IO format	WNRZ, WRZ, 0, 1
Pin or data multiplex:	Not support

7. Programmable clock generator:

Resource number:	4 clock/board
Input clock source:	Shared from free run clock
Output frequency:	1hz~200Mhz,
Period Jitter :	±150ppm
output frequency calculate by:	f(out)=f(in)*M/N/P M=2~32, N=2~32, P=1~65536 f(in)=free run clock

The MXLPC (64 IO Pin) AC Specification Summary (Continue)

8. Time and frequency measurement unit:

Number of measurement unit:	8 unit / Board
Per pin measurement:	Yes,
Maximum Frequency measurement:	400Mhz
Maximum Time measurement:	40sec(0.025Hz) Measurement resolution : 10ns
Input stage:	Embedded in IO pin PE Followed by Compare level (VOH/VOL)
Edge transient detect mode:	Normal level mode: by VOL Schmitt trigger mode: by VOL & VOH
Trigger Mode	micro-instruction, or CPU
Measurement counter size	Time:32 bits Frequency: 50 bits
Frequency measurement accuracy:	10ppm (typical)
Signal Shot Time measurement mode	Pulse low, Pulse high, Cycle

The MXLPC DC specification summary

1. Pin Driver Part

Driver Rise Time/Fall Time	1.4 V/1ns (measurement at VIH=3V, VIL=0V, un-terminated; 10% to 90%)
Output voltage range	VIH : -1.9V to +6.0V VIL : -2.0V to +5.9V
Output voltage precision	+/- (0.5%+20mV)
Output voltage resolution	0.61mV
Output current limit	75mA
Output voltage amplitude	0.05Vp-p to 8.0Vp-p
Output impedance	50±5Ω
I/O switching ON time	7ns (Typical)
I/O switching OFF time	5ns (Typical)

2. Comparator Part

Input voltage range	-2.0V to +6.0V
Input compare precision	+/- (0.5%+20mV)
Input voltage resolution	0.61mV
Input voltage amplitude	+/- 0.1 to +/- 8V
Input resistance/capacity	10MΩ or more / 50+/-15pF
Comparator switching time	2ns

3. Programmable Active Load

Current range	IOH: 0mA to –12mA IOL: 0mA to +12mA
Current resolution	1.464uA
Current accuracy	+/- (0.5%+25uA)
VREF assigned range	-1.75V to +5.75V
VREF resolution	0.61mV
VREF accuracy	+/- (0.5%+20mV)
Minimum ON time	11ns
Minimum OFF time	8ns

4. Programmable clamp

Clamp voltage	Clamp+:-1.5V to +6.0V, Clamp-:-2.0V to +5.0V
Clamp voltage precision	±(0.5%+50mV)
Clamp voltage resolution	0.61mV
Clamp current limit	60mA

The MXLPC DC specification summary (Continue)

5. HV Pin Driver Part (Per board 4channel)

Driver Rise Time/Fall Time	30mV/ns
Output voltage range VIH VIL VHH	 -0.1V to +6V -0.1V to +6V +5.9V to +13.5V
Output voltage precision	+/- (0.5%+20mV)
Output voltage resolution VIH VIL VHH	 0.61mV 0.61mV 1.22mV
Output Resistance	1 ohm (Typ), 10 ohm(Max)
Output current capability	60mA

6. PPMU (16 Bits DAC & 16 Bits ADC)

6.1. Forcing voltage:

force voltage Range	Range	Resolution	Max Current	Accuracy
-2V~+6V	2uA 20uA, 200uA 2mA 32mA	152uV	±2uA ±20uA ±200uA ±2mA ±32mA	+/- (0.1% + 5mV)

6.2. Force current:

Range	force current range	Resolution	Max. Current	Compliance Voltage range	Accuracy
±2uA	-2uA~ +2uA	122pA	±2.2uA	-2~+6V	±(0.2% + 10nA)
±20uA	-20uA~ +20uA	1.22nA	±22uA	-2~+6V	±(0.2% + 100nA)
±200uA	-200 A~ +200uA	12.2nA	±220uA	-2~+6V	±(0.2% + 1uA)
±2mA	-2m A~ +2mA	122nA	±2mA	-2~+6V	±(0.2% + 10uA)
±32mA	-32m A~ +32mA	1.52uA	±32mA	-2~+6V	±(0.2% + 100uA)

The MXLPC DC specification summary (Continue)

6.3. Measure voltage specification:

Range	Measure range	Resolution	Accuracy
-2V~+6V	-2V~+6V	152uV	±0.1%±10mV

6.4. Measure current specification:

Range	Measure range	Resolution	Accuracy
±2uA	-2uA ~ +2uA	61pA	±(0.2% + 10nA)
±20uA	-20uA ~ +20uA	610pA	±(0.2% + 100nA)
±200uA	-200uA ~ +200uA	6.1nA	±(0.2% + 1uA)
±2mA	-2mA ~ +2mA	61nA	±(0.2% + 10uA)
±32mA	-32mA ~ +32mA	984nA	±(0.2% + 100uA)

The MXLPC HSTMU specification

1. Configuration:

Configuration	Re-configure from MXLPC IO pin board
Pin number per board	32,64 pins per board, programmable
Controller:	Sequence Controller (MXPG3)
Log Trigger:	Pattern micro-instruction (UI) trigger, or Host CPU trigger
Working scheme	High resolution capture memory Waveform analysis approach.

2. Time and frequency measurement unit:

Number of measurement unit:	64 channels / Board 32 channels / Group
Input stage:	Embedded in IO pin PE Followed by Compare level (VOH/VOL)
Maximum input bandwidth :	400Mhz Followed by PE interface
Edge transient detect mode:	Normal level mode: by VOL Schmitt trigger mode: by VOL & VOH
Trigger Mode	micro-instruction, or CPU
Measurement mode	Frequency ,Pulse low, Pulse high, Cycle Rising edge, Falling edge
Capture memory	16K bits memory deep, Included PEL, PEH Log by change event or Continue.
Strobe resolution:	625 Pico-second
Time measurement maximum period	40 second

3. Others Specification:

- Please refer to MXLPC specification for detail DC specification.
- The IO pin AC function block is replaced with TMU function block.

  Others DC function block are still exist, ex: PMU, PPMU, Levels, DCL relay, etc.
- While re-configuration, each 16 pins are in a group, but any pin can be any site.
- Properly 3380 CRAFT statement supported and also raw capture data interface for user's application software.

The MXDPS (Device Power Supply) specification

1. Configuration:

Channel number:	8 channel / Board, 1 board / System (Default)
V range:	4V, 8V, 12V, 16V
I range:	1uA, 10uA, 100uA, 1mA, 10mA, 100mA, 1A, 2A
Outlet:	Go through pogo pin directly to load board
Measurement Trigger by:	CPU, Pattern
Function:	Force V, Force I , Measure I , Measure V, Clamp I , Clamp V, Constant current load, Clamp flag

2. Force V specification (16 bit DAC):

Range	Output voltage	Resolution	Max current	Accuracy
4V	-4V ~ +4V	0.1272mV	+/- 2 A	+/-(0.1%+1mV)
8V	-8V ~ +8V	0.2543mV	+/- 2 A	+/-(0.1%+2mV)
12V	-8V ~ +12V	0.3815mV	+/- 2 A	+/-(0.1%+3mV)
16V	-8V ~ +16V	0.5088mV	+/- 1.8 A	+/-(0.1%+4mV)

3. Force I specification (16 bit DAC):

Range	Max current	Resolution	Accuracy
100uA	-100uA ~ +100uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.00mA ~ +1.00mA	38.1nA	+/-(0.1% +1uA)
10mA	-10.0mA ~ +10.0mA	381nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.0A ~ +1.0A	38.1uA	+/-(0.1% +1mA)
2A	-2A ~ +2A	72.2uA	+/-(0.1% +2mA)

4. Measure I (18 bit ADC):

Range	Measuring	Resolution	Accuracy
1uA	-1.0uA ~ +1.0uA	11.7pA	+/-(0.1% +5nA)
10uA	-10.0uA ~ +10.0uA	117pA	+/-(0.1% + 10nA)
100uA	-100uA ~ +100A	1.17nA	+/-(0.1% + 100nA)
1mA	-1.00mA ~ +1.00mA	11.7nA	+/-(0.1% + 1uA)
10mA	-10.0mA ~ +10.0mA	117nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	1.17uA	+/-(0.1% + 100uA)
1A	-100A ~ +1.00A	11.7uA	+/-(0.1% +1mA)
2A	-2.00A ~ +2.00A	23.4uA	+/-(0.1% +2mA)

The MXDPS (Device Power Supply) specification (Continue)

5. Measure V (18bit ADC)

Range	Output voltage	Resolution	Accuracy
4V	-4.0V ~ +4.0V	31.25uV	+/-(0.1%+1mV)
8V	-8.0V ~ +8.0V	62.5uV	+/-(0.1%+2mV)
12V	-12.0V ~ +12.0V	93.75uV	+/-(0.1%+3mV)
16V	-16.0V ~ +16.0V	125uV	+/-(0.1%+4mV)

6. Clamp I (over current clamp & under current clamp), (16bit ADC) :

Range	Max current	Resolution	Accuracy
100uA	-125uA ~ +125uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.25mA ~ +1.25mA	38.1nA	+/-(0.1% +1uA)
10mA	-12.5mA ~ +12.5mA	381nA	+/-(0.1% + 10uA)
100mA	-125mA ~ +125mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.25A ~ +1.25A	38.1uA	+/-(0.1% +1mA)
2A	-2.5A ~ +2.5A	72.2uA	+/-(0.1% +2mA)

7. Clamp V:

Range	Output voltage	Resolution	Accuracy
16V	-8V ~ +16V	0.515mV	+/-(0.1%+4mV)

8. Constant current load:

Range	Max current	Resolution	Accuracy
100uA	-100uA ~ +100uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.0mA ~ +1.0mA	38.1nA	+/-(0.1% +1uA)
10mA	-10.0mA ~ +10.0mA	381nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.0A ~ +1.0A	38.1uA	+/-(0.1% +1mA)
2A	-2.0A ~ +2.0A	72.2uA	+/-(0.1% +2mA)

9. Settling timing specification for voltage force

Range	Settling Time @ Normal Rate Mode	Settling Time @ Fast Rate Mode
4V	500uS	6us
8V	550uS	6.5us
12V	600uS	7us
16V	650uS	7.5us

Note: 1.Settling time measurement at 99% accuracy.

The MXDPS (Device Power Supply) specification (Continue)

10. Special digital support:

- Data log memory: 512K*32 bits, general-purpose.
- Pattern synchronization operation: TBD.

The MLDPS (Device Power Supply) specification summary

1. Configuration:

Number of channel:	32 channel / board
FUNCTIONS	FVMI, FIMV, FNMV, Clamp I, Clamp V, Gang mode
Force V range:	12V, 6V(Only 6V range support 1A I range)
Measure I range:	5uA, 25uA, 250uA, 2.5mA, 25mA, 500mA, 1A
Force I range	25mA, 500mA, 1A
Measure V range	12V
Gang mode support:	500mA & 1A in parallel mode
Outlet:	Go through pogo pin directly to load board
Measurement Trigger by:	CPU, Pattern
Over Temp Protection:	Thermal shutdown

2. Force V (16 bits DAC):

Range	Output voltage	Resolution	Max current	Accuracy
12V	-6V~+12.5V	0.39mV	+/- 500mA	+/-(0.05%+2mV)
6V	-6V~+6V	0.39mV	+/- 1A	+/-(0.05%+2mV)

Note: The different V range provide different output current, but same resolution and accuracy.

3. Force I (16 bits DAC):

Range	Max current	Resolution	Accuracy
25mA	-25.625m A ~ +25.625m A	782nA	+/-(0.05% + 12.5uA)
500mA	-512.5m A ~ +512.5m A	31.28uA	+/-(0.05% +1mA)
1A	-1.025 A ~ +1.025 A	31.28uA	+/-(0.05% +1mA)

Note: The 1A range had limited output voltage to +/-5V only.

4. Measure V (18 bits ADC):

Range	Output voltage	Resolution	Accuracy
12V	-12.5V ~ +12.5V	93.75uV	+/-(0.05%+2mV)

The MLDPS (Logic Device Power Supply) specification summary

5. Measure I (18 bits ADC):

Range	Max current	Resolution	Accuracy
5uA	-5u A ~ +5u A	38.1pA	+/-(0.1% + 5nA)
25uA	-25u A ~ +25u A	190pA	+/-(0.1% +25nA)
250uA	-250u A ~ +250u A	1.9nA	+/-(0.1% + 250nA)
2.5mA	-2.5m A ~ +2.5m A	19uA	+/-(0.1% + 2.5uA)
25mA	-25m A ~ +25m A	190uA	+/-(0.1% + 25uA)
500mA	-500mA ~ +500mA	15.24uA	+/-(0.1% +1mA)
1A	-1A ~ +1A	15.24uA	+/-(0.1% +1mA)

6. Clamp I (over/under current clamp) (16bit DAC):

Range	Max current	Resolution	Accuracy
250uA	-256.25u A ~ +256.25u A	7.82nA	+/-(0.2% + 1.25uA)
2.5mA	-2.5625m A ~ +2.5625m A	78.2nA	+/-(0.2% + 12.5uA)
25mA	-25.625m A ~ +25.625m A	782nA	+/-(0.2% + 125uA)
500mA	-512.5m A ~ +512.5m A	15.7uA	+/-(0.2% +5mA)
1A	-1.025 A ~ +1.025 A	30.14uA	+/-(0.2% +5mA)

PS. Clamp I value can't setup less than 10% of I range value.

7. Clamp V (16 bit DAC):

Range	Output voltage	Resolution	Accuracy
12V	1.25V~12.5V -1.25V~12.5V	0.39mV	+/-(0.2%+5mV)

8. Gang mode:

- Maximum channels at gang mode are constant 32 channels.

The MXPMU (Precision Measurement Unit) specification summary

1. Configuration:

Number of channel:	16 channel / board
Number of board in a system:	3380P: 1 board / system 3380: 2 board / system
Number of V range:	6V, 12V, 24V, 48V,
Number of I range:	1uA, 10uA, 100uA, 1mA, 10mA, 100mA
Outlet:	Go through pogo pin of ATE tester pin
Measurement Trigger by:	CPU
DAC and ADC chip:	16 bits
Clamp:	Programmable

2. V_RANGE specification:

V_Range	Resolution	Accuracy
+/- 6V	250uV	+/- (0.1% + 5mV)
+/- 12V	500uV	+/- (0.1% + 10mV)
+/- 24V	1mV	+/- (0.1% + 20mV)
+/- 48V	2mV	+/- (0.1% + 40mV)

3. I_RANGE specification

I_Range	Resolution	Accuracy
+/- 1uA	40pA	+/- (0.2% + 5nA)
+/- 10uA	400pA	+/- (0.2% + 50nA)
+/- 100uA	4nA	+/- (0.2% + 500nA)
+/- 1mA	40nA	+/- (0.2% + 5uA)
+/- 10mA	400nA	+/- (0.2% + 50uA)
+/- 100mA	4uA	+/- (0.2% + 500uA)

4. Slew rate and settling specification

V_Range	Slew rate	Settling time
+/- 6V	2.5V/mS	4.5mS
+/- 12V	5V/mS	4.5mS
+/- 24V	10V/mS	6mS
+/- 48V	20V/mS	6mS

Note: 1. Slew rate test condition: current range @10mA, no load, 5%~95% of voltage force at full range.
2. Settling time test condition: current range @10mA, no load, 99.5% accuracy

The MXREF (Reference Power Source) specification summary

1. Configuration:

Number of channel:	16 channels per board
Number of board in a system:	optional
V range:	6V, 12V, 24V, 48V
I range:	1uA, 10uA, 100uA, 1mA, 10mA,100mA,250mA
Outlet:	Go through pogo pin directly
Current gang support	Yes, maximum 4 channels gang on each group
Measurement Trigger by:	By CPU Trigger, or By pattern
DAC and ADC chip:	16 bits
Clamp:	Programmable

2. V_RANGE specification:

Voltage Range Name	Voltage Output Maximum	Resolution	Accuracy
6V	+/- 6V	250uV	+/- (0.1% + 4mV)
12V	+/- 12V	500uV	+/- (0.1% + 8mV)
24V	+/- 24V	1mV	+/- (0.1% + 16mV)
48V	+/-48V/Max.100mA +/-45V/Max.250mA (Note1)	2mV	+/- (0.1% + 32mV)

Note: 1. Refer to Operating V/I curve. For detail

3. I_RANGE specification

I_Range	Resolution	Accuracy	NOTES
+/-1uA	40pA	+/- (0.2% + 5nA)	
+/- 10uA	400pA	+/- (0.2% + 50nA)	
+/- 100uA	4nA	+/- (0.2% + 500nA)	
+/- 1mA	40nA	+/- (0.2% + 5uA)	
+/- 10mA	400nA	+/- (0.2% + 50uA)	
+/- 100mA	4uA	+/- (0.2% + 500uA)	
+/- 250mA	10uA	+/- (0.2% + 1.5mA)	

4. Current gang specification

Channel group on gang mode	channel 0~3, 4~7, 8~11, 12~15
Gang mode channel selection	continued 2, 3, or 4 channels in each group, maximum 4 channels

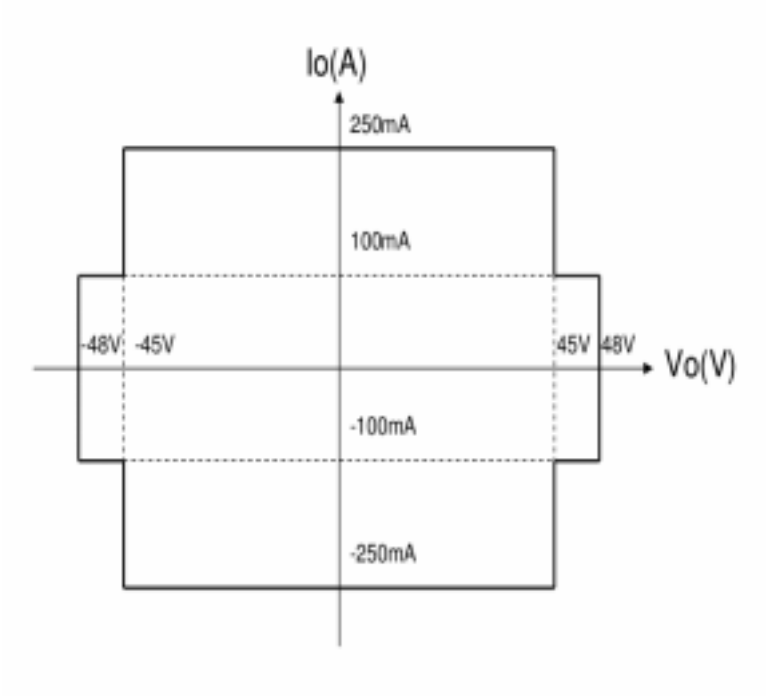
The MXREF (Reference Power Source) specification summary

5. Slew rate and settling specification

Voltage Range Name	Slew Rate @ Normal Mode	Slew Rate @Fast Mode	Settling Time @ Normal Mode	Settling Time @Fast Mode
6V	2.5V/mS	9V/mS	4.5mS	3mS
12V	5V/mS	18V/mS	4.5mS	3mS
24V	10V/mS	36V/mS	6mS	3mS
48V	20V/mS	72V/mS	6mS	3mS

Note: 1. Slew rate test condition: current range @10mA, no load, 5%~95% of voltage force at full range.
2. Settling time test condition: current range @10mA, no load, 99.5% accuracy.
3. Faster slew rate will cause more ripple at output while clamped.

6. Operating V/I curve



The MXUVI (Universal Voltage/Current Source) specification summary

1. Configuration:

Number of channel:	16 channels per board
Number of board in a system:	optional
V range:	2V, 4V, 6V, 12V
I range:	1uA, 10uA, 100uA, 1mA, 10mA,100mA, 1A
Outlet:	Go through pogo pin directly
Current gang support	Yes, maximum 4 channel gang on each group
Measurement Trigger by:	By CPU Trigger, or By pattern
DAC and ADC chip:	16 bits
Clamp:	Programmable

2. Voltage Range Specification:

Voltage Range Name	Voltage Output Maximum	Resolution	Accuracy
2V	+/- 2V	75uV	+/- (0.1% + 1.75mV)
4V	+/- 4V	150uV	+/- (0.1% + 3.5mV)
6V	+/- 6V	225uV	+/- (0.1% + 5mV)
12V	+/- 12V	450uV	+/- (0.1% + 10mV)

3. Current Range Specification:

I_Range	Resolution	Accuracy	NOTES
+/-1uA	40pA	+/- (0.2% + 5nA)	
+/- 10uA	400pA	+/- (0.2% + 50nA)	
+/- 100uA	4nA	+/- (0.2% + 500nA)	
+/- 1mA	40nA	+/- (0.2% + 5uA)	
+/- 10mA	400nA	+/- (0.2% + 50uA)	
+/- 100mA	4uA	+/- (0.2% + 500uA)	
+/- 1A	40uA	+/- (0.2% + 5mA)	

4. Current gang specification

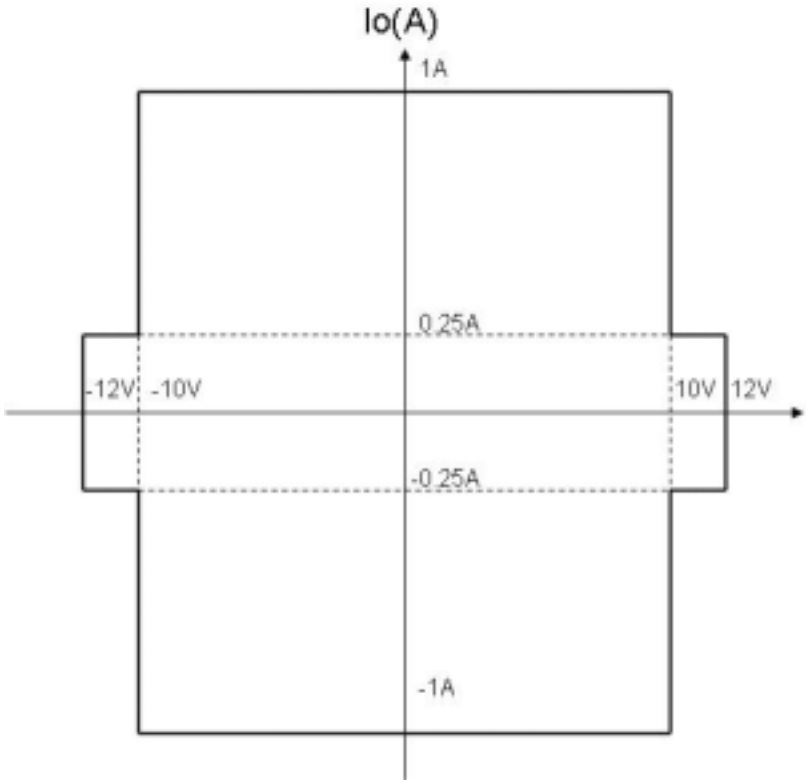
Channel group on gang mode	channel 0~3, 4~7, 8~11, 12~15
Gang mode channel selection	continued 2, 3, or 4 channels in each group, maximum 4 channels

5. Slew rate and settling specification

Voltage Range Name	Slew Rate @ Normal Mode	Slew Rate @Fast Mode	Settling Time @ Normal Slew Rate Mode	Settling Time @Fast Slew Rate Mode
2V	3V/mS	12.5V/mS	1.6mS	450uS
4V	6V/mS	25V/mS	1.6mS	450uS
6V	9V/mS	37.5V/mS	1.6mS	450uS
12V	18V/mS	75V/mS	1.6mS	450uS

Note: 1. Slew rate test condition: current range @10mA, no load, 5%~95% of voltage force at full range.
2. Settling time test condition: current range @10mA, no load, 99.5% accuracy.
3. Faster slew rate will cause more ripple at output while clamped.

6. Operating V/I curve



The MXAWI (ADDA) specification summary

1. Feature:

1. 4 channels waveform generator, and 4 channels waveform digitizer
2. 50 MHz with 16 bits arbitrarily waveform generator.
3. The Chroma 3380 Craft software supported on test plan, test pattern, and GUI utilities.
4. Fully pattern synchronization trigger working scheme.
5. Shared with the common slot.

2. WG (Waveform Generator) Specification:

Resolution	16 bits
Monotonicity	14 bits
Conversion rate	50 MSPS
Waveform memory	256K
Waveform setting time	1uS
Output voltage range:	+/-2.5V on LV(Low Voltage Range) +/-10V on HV(High Voltage Range) (default)
Output voltage Accuracy:	0.5 mV on LV(Low Voltage Range) 1.5 mV on HV(High Voltage Range)
Output current	10mA
Output voltage range	+/- 2.5V; +/- 10V(default)
Output mode	Single end or Differential
Output filter	20K , Through
Trigger method,	By pattern, 8M pattern memory depth
Waveform offset DAC resolution	16 bits
Offset voltage range	-10.0V ~ +10.0V
Default common mode voltage	0.0V

3. WD (Waveform Digitizer) specification:

Waveform capture ADC resolution	16 bits
Conversion rate	250 KSPS
Capture memory	256K
Input voltage range	+/- 10.0 V; +/- 2.5 V(Default)
Input mode	Single end or Differential
filter	20K , 50K , Through
Trigger method,	By pattern, 8M pattern memory depth
Waveform offset DAC resolution	16 bits
Offset voltage range	-10.0V ~ +10.0V
Default common mode voltage	0.0V
Voltage Measurement Accuracy:	1.5 mV on LV(Low Voltage Range) 2.5 mV on HV(High Voltage Range)

The MAWI2 (ADDA) specification summary

1. Feature

1. 4 channels waveform generator and 4 channels waveform digitizer.
2. 384 kHz with 24 bits arbitrarily waveform generator.
3. 2.5MHz with 24bit waveform digitizer.
4. The Chroma 3380 Craft software supported on test plan, test pattern, and GUI utilities.
5. Shared with the common slot.

2. WG(Waveform Generator) Specification:

General Specification

WG channels	4
DAC Resolution	24bit
Conversion rate	48 kS/s audio system: 384 kS/s, 192 kS/s, 96 kS/s, 48 kS/s, 32 kS/s, 16kS/s, 8 kS/s 44.1 kS/s audio system: 176.4 kS/s, 88.2 kS/s, 44.1 kS/s
Output current	+/-40mA min
Output mode	Single ended, Differential
Waveform memory	512K(each channel)

Output Voltage specifications

Range	Voltage Span	Output Voltage	Resolution	Accuracy
+/-8V	8Vpp	+8V~-8V	1.3uV	+/-(0.1%+2mV)
+/-2.5V	5Vpp	+5V~-5V	325nV	+/-(0.1%+1mV)

Programmable DC offset

Voltage Range	+/-8V Range :+8V ~ -8V +/-2.5V Range :+5V ~ -5V
Resolution	0.305mV
Accuracy	+/-(0.1%+1mV)

Output impedance

50 ohm mode	50ohm
Low Z mode	<2 ohm

The MAWI2 (ADDA) specification summary (continue)

Analog Anti-imaging Filters

Filter selectable	-3db Frequency	Filter type
24kHz filter	24kHz	Butterworth
100kHz filter	100kHz	Butterworth

AC performance

Output Frequency range	Anti-image Filter Selected	THD	SFDR	SNR
100Hz-1kHz	Bypass	93db	95db	93db
100Hz-1kHz	24kHz	90db	95db	94db
100Hz-24kHz	100kHz	TBD	TBD	TBD

3. WD (Waveform Digitizer) specification:

General Specification

WD channels	4
ADC resolution	2.5 MS/s 24bits Sigma-Delta ADC
Effective bits	20 MS/s :12bits 5 MS/s :16bits Under 2.5 MS/s :24bits
Sampling rate	High precision mode General frequency: 2.5 MS/s, 1.25 MS/s, 625 kS/s, 312.5 kS/s, 156.25 kS/s, 78.125 kS/s 48ks/s audio system: 1.536 MS/s, 768 kS/s, 384 kS/s, 192 kS/s, 96 kS/s, 48 kS/s 44.1kS/s audio system: 1.4112 MS/s, 705.6 kS/s, 352.8 kS/s, 176.4 kS/s, 88.2 kS/s, 44.1kS/s High speed mode 20 MS/s, 5 MS/s Universal mode 2.5 MS/s~ 62.5 KS/s with 20ns resolution
Input mode	Single ended, Differential
Capture memory	512K(each channel)

Input Voltage Specification

Range	Voltage Span	Output Voltage	Resolution	Accuracy
+/-8V	8Vpp	+8V~-8V	1.3uV	+/-(0.1%+2mV)
+/-2.5V	5Vpp	+5V~-5V	325nV	+/-(0.05%+1mV)

The MAWI2 (ADDA) specification summary (continue)

Programmable DC offset

Range	+/-8V Range :+8V ~ -8V +/-2.5V Range :+5V ~ -5V
Resolution	0.305mV
Accuracy	+/-(0.1%+0.5mV)

Input impedance

High impedance mode	>1M ohm
Single ended terminated mode	50 ohm+/-2 ohm
Differential terminated mode	100 ohm+/-4ohm

Analog Anti-aliasing Filters

Filter selectable	-3db Frequency	Filter type
24kHz filter	24kHz	Butterworth
100kHz filter	100kHz	Butterworth

AC performance

Output Frequency range	Anti- aliasing Filter Selected	THD	SFDR	SNR
100Hz-1kHz	Bypass	94 db	95 db	94 db
100Hz-1kHz	20kHz	94 db	95 db	94 db
100Hz-24kHz	100kHz	TBD	TBD	TBD

The MXBUS board:

- The communication interface board for host PC and test head.
- System power on/off control.
- System monitor, include DC power level, fan status, and vacuum status (3380 only).
- 64 channels of user relay control (URC) signals.
- Serial relay interface, expandable number by user.
- User relay power outlet: 5V/4A, with over current protection.
- Auxiliary power for load board: 5V/2A with short protection (MXBUS).
- Auxiliary power for load board: +/-15V/1A with short protection.(MXPG3)

The STPCI board:

- The interface board between host PC and test head.
- The PCI 2.1a or higher specification compliant.
- The dual LVDS cables as link between STPCI and test head SPBUS.

The STPHI Board:

- The TTL level prober and handler interface board, defined as option on system.
- Maximum 4 sites support, and maximum 32 bits bin data.
- Single or multiple SOT (start of test) test start protocol support.
- Parallel or serial, binary or one hot bin data format.
- Selectable active high or low for all signals.
- Interface timing resolution=1us, setting range > 100 sec..

The PXI extension carriage board:

1. Configuration:

- MXPXI →Carriage board converts a PXI system slot to a standard 3U PXI add on card,